1. See something like “Cannot assign a packed type 'bit[11:0]' to an unpacked type 'reg $[Bits-1:0]'”
   1. Issue: Packed Vs. Unpacked Array
   2. How to fix it:
      1. Look for where you declared your variables and see what your ordering of vector vs. name is
      2. Packed = In[0:1]
      3. Unpacked = [0:1] In
2. Use Run -100 for simulation, Run - all may just freeze simulation
3. Issue: Full netlist not showing up on waveform
   1. How to fix it: When optimizing go to Optimization Options and make sure on the farthest left tab you select Apply full visibility to all modules
4. Not getting expected output
   1. Issue: running simulation on testbench and module
   2. How to fix it: Only run your simulation on the testbench as it is calling an instantiation of the module